

REMARKS/ARGUMENTS

Examiner Nguyen is thanked for the thorough examination of the subject Patent Application. The Claims have been carefully reviewed and amended, and are considered to be in condition for allowance.

5 Reconsideration of the objection to the amendment filed 1/14/05 under 35 U.S.C. §132 because it introduces new matter into the disclosure of the invention. The applicant believes that added material is not new matter. The original text describes that:

10 “Because of its large coupling ratio, CHC essentially charge couples the VB11 gate voltage of the PMOS bias node, to the VSS source voltage...”
(Page 5, last paragraph, lines 2-4)

Employing basic electronic principles, the large coupling ratio provides a charge coupling or AC coupling of the biasing voltage VB11 at the bias node b11 to the lower supply voltage VSS. Thus the coupling ratio would be defined as:

$$\begin{aligned} CR &= \frac{VB11}{VSS} = \frac{VSS \frac{Z_{CP}}{Z_{HC} + Z_{CP}}}{VSS} = \frac{Z_{CP}}{Z_{HC} + Z_{CP}} \\ &= \frac{1}{\frac{j\omega C_P}{1} + \frac{1}{j\omega C_{HC}}} = \frac{C_{HC}}{C_{HC} + C_P} \end{aligned}$$

Where:

$$Z_{CP} = \frac{1}{j\omega C_P},$$

$$Z_{HC} = \frac{1}{j\omega C_{HC}}, \text{ and}$$

$$V_{B11} = V_{CP} = V_{SS} \frac{Z_{CP}}{Z_{HC} + Z_{CP}}.$$

5 It can be shown that as the magnitude of the capacitance of the large capacitor C_{HC} relative to the capacitance of the parasitic capacitor C_P grows larger, any noise voltage present on the lower supply voltage V_{SS} is charge coupled or AC coupled directly to the bias node **b11**. Further it is apparent that the larger magnitude of the capacitance of the large capacitor C_{HC} relative to the
10 capacitance of the parasitic capacitor C_P , the coupling ratio approaches unity (1).

The applicant requests that the clean version of the specification as presented in the appendix of this amendment be entered as conforming to 37 CFR 1.125(b) and (c). As explained in detail above, the specification contains no new matter. The clean version of the specification as presented in this
15 amendment shows the amendment to the specification and the Claims as shown above.

Reconsideration of the objection to Claims 1-42 because of informalities is requested. Claims 1-42 are amended to provide correct description of the elements and function of the elements as requested by the Examiner.

Reconsideration of the rejection under 35 USC §112, first paragraph of
5 Claims 1-42 for failing to comply with the written description requirements, in that the claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor at the time of the application was filed, had possession of the claimed invention is requested in light of the following arguments.

10 The original text describes that:

“Because of its large coupling ratio, CHC essentially charge couples the VB11 gate voltage of the PMOS bias node, to the VSS source voltage...”
(Page 5, last paragraph, lines 2-4)

Employing basic electronic principles, the large coupling ratio provides a
15 charge coupling or AC coupling of the biasing voltage VB11 at the bias node b11 to the lower supply voltage VSS. Thus the coupling ratio would be defined:

$$\begin{aligned} CR &= \frac{VB11}{VSS} = \frac{VSS \frac{Z_{CP}}{Z_{HC} + Z_{CP}}}{VSS} = \frac{Z_{CP}}{Z_{HC} + Z_{CP}} \\ &= \frac{\frac{1}{j\omega C_P}}{\frac{1}{j\omega C_{HC}} + \frac{1}{j\omega C_{HC}}} = \frac{C_{HC}}{C_{HC} + C_P} \end{aligned}$$

Where:

$Z_{CP} = \frac{1}{j\omega C_P}$ is the impedance of the parasitic capacitance C_P .

5 $Z_{HC} = \frac{1}{j\omega C_{HC}}$ is the impedance of the very large capacitance C_{HC} .

$VB11 = V_{CP} = VSS \frac{Z_{CP}}{Z_{HC} + Z_{CP}}$ is the voltage

VB11 present at the node b11 and can be found as a voltage divider of the impedance

10 Z_{HC} of the very large capacitor C_{HC} and the impedance Z_{CP} of the parasitic capacitor C_P as shown.

It can be shown that as the magnitude of the capacitance of the large capacitor C_{HC} relative to the capacitance of the parasitic capacitor C_P grows larger, any noise voltage present on the lower supply voltage V_{SS} is charge coupled or AC coupled directly to the bias node b11. Further it is apparent that the larger
5 magnitude of the capacitance of the large capacitor C_{HC} relative to the capacitance of the parasitic capacitor C_P , the coupling ratio approaches unity (1).

The concept of coupling ratio is not new in the art, as shown in Silicon Processing for the VLSI Era, Volume II Process Integration, Wolf, Lattice Press, Sunset Beach, CA., 1990, pp: 623-627. In nonvolatile or Flash memory the
10 capacitive coupling coefficient of the capacitance of the control gate to the floating gate of the nonvolatile memory cell and the capacitance of the floating gate of the nonvolatile memory cells to the bulk semiconductor substrate of a nonvolatile memory cell, the coupling coefficient is used to determine the amount of charge coupled to the floating gate to determine the necessary programming
15 voltages and the time for programming the nonvolatile memory cell. The serial structure of the floating gate nonvolatile memory employs similar concepts to the present invention. The very large capacitor C_{HC} in series with the parasitic capacitor C_P as shown in Fig. 4a demonstrates that the large value of capacitance of the very large capacitor C_{HC} relative to the parasitic capacitor C_P
20 causes the voltage V_{B11} at the node b11 is essentially equal to the lower supply voltage V_{SS} and the coupling ratio approaches one (1) as shown above.

Reconsideration of the rejection under 35 USC §112, second paragraph, of Claims 1-42 as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention is requested in light of the following arguments.

5 Claims 1, 12, 23, and 33 are amended to more clearly define the coupling ratio of the very large capacitor C_{HC} and the parasitic capacitor C_P as “approximately equal to a unity value”. Claims 9, 20, 30, and 40 are amended to state that “the third transistor and the fourth transistor activate and deactivate almost simultaneously as determined by said input signal”.

10 In Claims 10, 21, 31, and 41, the charge coupling is defined as an AC coupling as stated in amended paragraph [0019]. The original specification stated that:

“Because of its large coupling ratio, C_{HC} essentially charge couples the VB11 gate voltage of the PMOS bias node, to the VSS source voltage...”

15 (Page 5, last paragraph, lines 2-4)

This “charge coupling” of the gate of the PMOS bias node to the VSS source voltage is an AC coupling to minimize the impact of AC noise on the bias voltage VB11.

Claims 11, 22, 32, 42 are amended to "the capacitance value of the large capacitor is chosen to be very large with respect to a capacitance value of said parasitic capacitor" to make the definition of the magnitude of the very large capacitor C_{HC} versus the parasitic capacitor C_P .

5 Claims 12 and 23 are amended to provide correct antecedent basis.

Claim 33 is amended to definitely define the "apparatus comprising".

Reconsideration of the rejection under 35 USC §103(a) of Claims 1-42 as being unpatentable over in Applicant's Admitted Prior Art (AAPA) in view of U. S. Patent 6,373,328 (Rapp) is requested in light of the following arguments.

10 While the AAPA does illustrate an input buffer receiver, it does not include the

a large capacitor coupled between the bias node and a lower supply voltage for providing a coupling ratio between said large capacitor and a parasitic capacitor coupled between said bias node and a ground reference point is approximately equal to a unity value such that a
15 biasing voltage at said biasing node follows said lower supply voltage to minimize effects of a ground noise signal between the lower supply voltage and the ground reference point; (Claim 1, Lines 4-10 and Claim 12, Lines 7-17)

forming a large capacitor coupled between the bias node and the lower
supply voltage for providing a coupling ratio between said large
capacitor and a parasitic capacitor coupled between said bias node
and a ground reference point is approximately equal to a unity value
such that a biasing voltage at said biasing node follows said lower
supply voltage to minimize effects of said ground noise between the
lower supply voltage and the ground reference point; (Claim 23, Lines
6-13)

and

means for forming a large capacitor between the bias node and the lower
supply voltage for providing a coupling ratio between said large
capacitor and a parasitic capacitor coupled between said bias node
and a ground reference point is approximately equal to a unity value
such that a biasing voltage at said biasing node follows said lower
supply voltage to minimize effects of said ground noise between the
lower supply voltage and the ground reference point; (Claim 33, Lines
8-15)

While Rapp does show “an n-type transistor 90” connected to serve “as a
capacitor, helping to hold the voltage constant at the gate of transistor 86” (Rapp,
Col 9, Lines 38-42). Rapp does not discuss:

An input buffer receiver comprising:

a buffer input portion for receiving an input signal, said buffer input portion comprising a bias node;

a large capacitor coupled between the bias node and a lower supply
5 voltage for providing a coupling ratio between said large capacitor and
a parasitic capacitor coupled between said bias node and a ground
reference point is approximately equal to a unity value such that a
biasing voltage at said biasing node follows said lower supply voltage
to minimize effects of a ground noise signal between the lower supply
10 voltage and the ground reference point; and

a buffer output portion in communication with the buffer input portion for
producing an output signal; (Claim 1, Lines 1-12 and Claim 12, Lines
4-19)

A method for minimizing effects of ground noise on an input buffer
15 receiver comprising the steps of:

forming a buffer input portion for receiving an input signal on a substrate;

forming a bias node within said buffer input portion;

connecting a lower supply voltage to said buffer input portion;

forming a large capacitor coupled between the bias node and the lower
supply voltage for providing a coupling ratio between said large
capacitor and a parasitic capacitor coupled between said bias node
and a ground reference point is approximately equal to a unity value
such that a biasing voltage at said biasing node follows said lower
supply voltage to minimize effects of **[[a]]** said ground noise between
the lower supply voltage and the ground reference point; and

forming a buffer output portion on said substrate in communication with
the buffer input portion for producing an output signal; (Claim 23, Lines
1-15)

An apparatus for minimizing effects of ground noise on an input buffer
receiver, said apparatus comprising:

means for forming a buffer input portion for receiving an input signal on a
substrate;

means for forming a bias node within said buffer input portion;

means for connecting said a lower supply voltage to said buffer input
portion;

means for forming a large capacitor between the bias node and the lower
supply voltage for providing a coupling ratio between said large
capacitor and a parasitic capacitor coupled between said bias node
and a ground reference point is approximately equal to a unity value
such that a biasing voltage at said biasing node follows said lower
supply voltage to minimize effects of **[[a]]** said ground noise between
the lower supply voltage and the ground reference point; and

means for forming a buffer output portion on said substrate in
communication with the buffer input portion for producing an output
signal. (Claim 33, Lines 1-18)

The large capacitor in Rapp is connected to the ground reference point and does
not charge couple the biasing node to the lower supply voltage such that the
voltage at the biasing node follows the lower supply voltage. Further, the circuit
of Rapp provides a comparator circuit that compares the voltage value of a
programming voltage supply V_{PP} at node A of Fig. 5 of Rapp against the voltage
value of the power supply voltage V_{DD} . The capacitor of Rapp helps "to hold the
voltage constant at the gate of transistor 86" this does not provide the coupling of
the lower supply voltage to the biasing node of this invention.

The invention as claimed in amended Claims 1-42 is believed to be novel
and patentable over AAPA in view of Rapp because there is not sufficient basis

for concluding that the combination of claimed elements would have been obvious to one skilled in the art. That is to say, there must be something in the prior art or line of reasoning to suggest that the combination of these various references is desirable. The applicant believes that there is no such basis for the combination. The applicant, therefore, request Examiner Nguyen reconsider his rejection in view of these arguments.

The applicant understands that Examiner's FINAL position re this office action and respectfully requests that a timely Notice of Allowance for all claims be issued in this case.

It is requested that should Examiner Nguyen not find that the Claims are now allowable, that the undersigned be called at (845) 452-5863 to overcome any problems preventing allowance.

Respectfully Submitted,
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